PLESSEY
Semiconductors

T-45-19-05

SP8643A

350MHz ÷ 10/11

The SP8643 is an ECL variable modulus divider, with ECL 10K compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

The two clock inputs are interchangeable and either will act as a clock inhibit when connected to an ECL high level. Normally, one input is left open circuit and the other is AC coupled, with externally-applied bias.

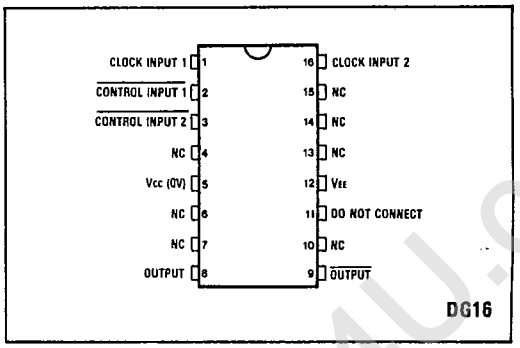


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Inputs/Outputs
- AC Coupled Input (External Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 260mW
- Temperature Range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

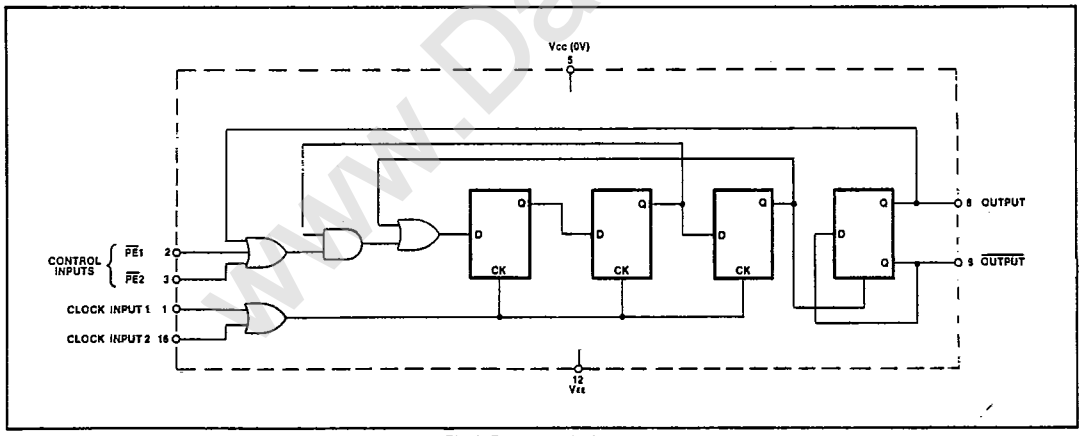


Fig.2 Functional diagram

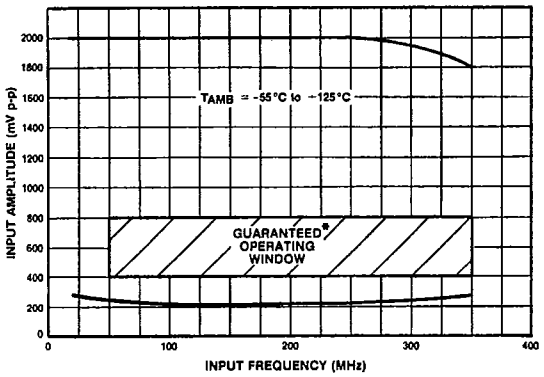
ELECTRICAL CHARACTERISTICS

T-45-19-05

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value Min.	Value Max.	Units	Conditions	Notes
Maximum frequency (sinewave input)	f_{max}	350		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to ECL output delay	t_p		6	ns		Note 6
Set-up time	t_s	2.5		ns		Note 6
Release time	t_r	3		ns		Note 6

NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L ⟶ H transition of control input and the next L ⟶ H clock pulse transition to ensure that ÷10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H ⟶ L transition of the control input and the next L ⟶ H clock pulse transition to ensure that the ÷11 mode is obtained.
6. Guaranteed but not tested.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8643A

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

OPERATING NOTES

1. The clock and control inputs are ECL III compatible. There is an internal pulldown resistor to V_{EE} of 4.3k on each input and therefore any unused input can be left open circuit when not in use but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity. If it is desirable to capacitively couple the signal source to the clock input then an external bias is required as shown in Fig. 6. The external bias voltage should be -1.3V at 25°C.
2. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. Input impedance is a function of frequency. See Fig. 5.
5. All components should be suitable for the frequency in use.

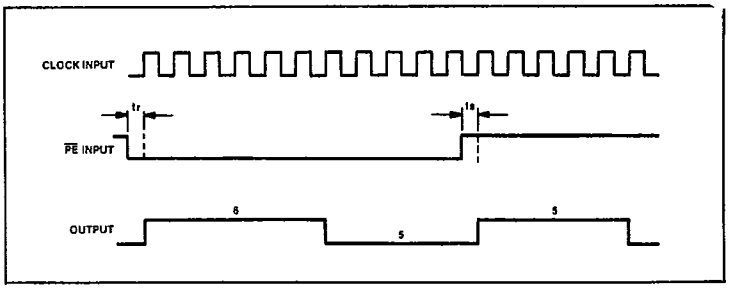


Fig.4 Timing diagram

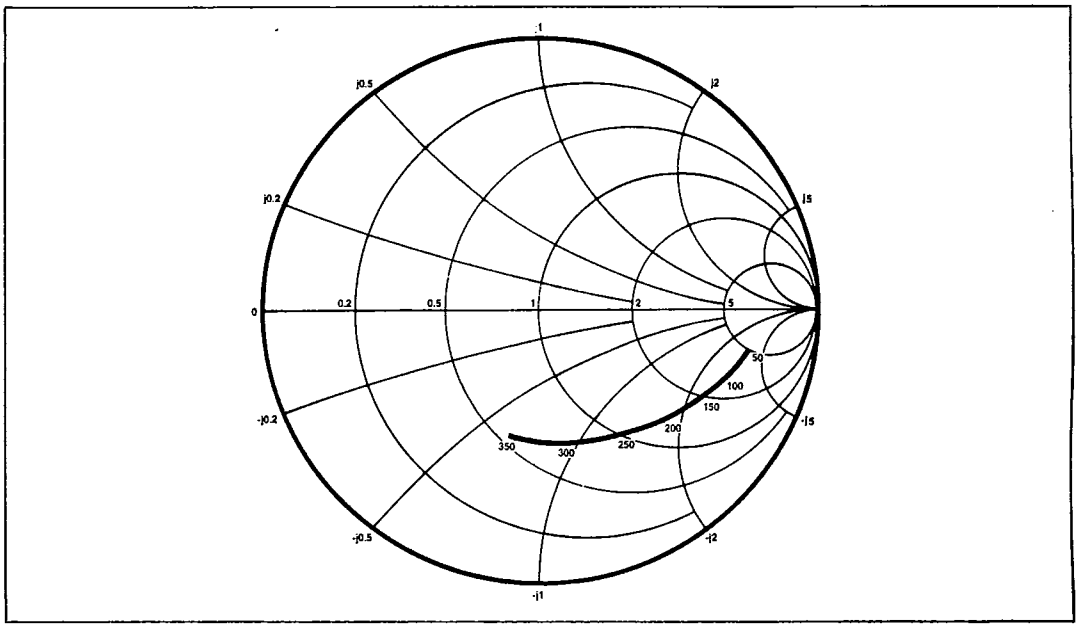


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

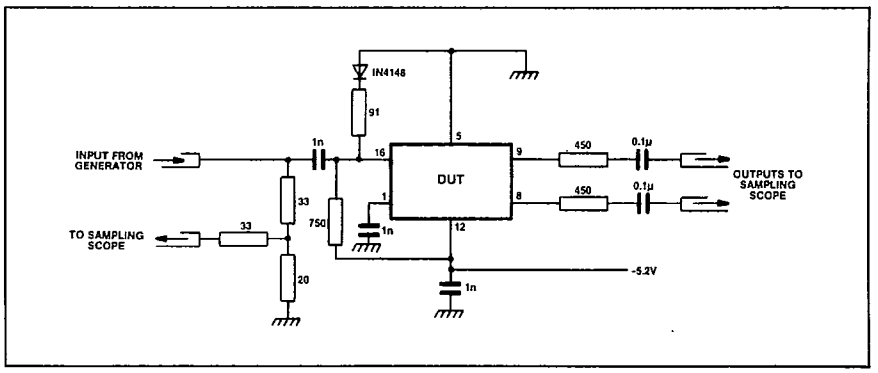


Fig.6 Test circuit

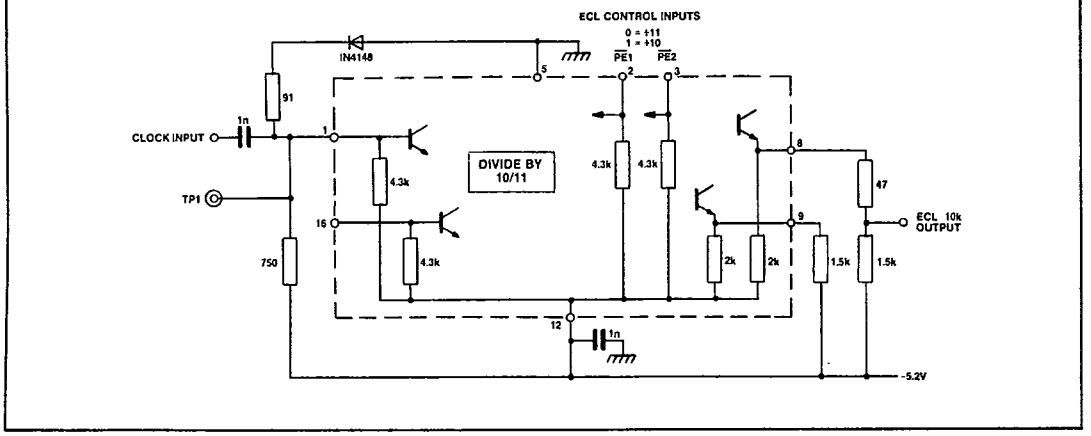


Fig.7 Typical application using ECL outputs. NB Voltage at TP1 should be -1.3V at 25°C